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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/980,098	03/15/2002	Shinji Itami	Q67475	1120

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2100 Pennsylvania Avenue NW
Washington, DC 20037-3213

EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/980,098	ITAMI, SHINJI	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,6 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 24th of September 2004. Claims 1 and 5 have been amended; claim 4 has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 24th of June 2004. Currently, claims 1, 3, 5, 6 and 8 are pending in this application.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 3 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims 1 and 5 fail to positively recite the boundaries sought for protection, respectively. The metes and bounds of the respective claim cannot be determined because it is unclear as to which category of subject matter is sought for protection, i.e., the method or the apparatus. In other words, the claim language does not adequately specify what is covered in its metes and bounds should it mature into a patent. It is essential that the Applicant makes clear what is covered by the claim in order to determine patentability. See *In re Steele, 49 CCPA 1295, 134 USPQ 292.*

The claim 3 is dependent claim of the claim 1.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1, 3, 5, 6 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art [hereinafter AAPA] in view of Oshikawa [JP 401173149 A; cited by the Applicant].

Referring to claim 1, AAPA discloses a data transmission system (Fig. 16) for carrying out data transmission/reception (See page 1, lines 16-20) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A 15:2/D 15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A 15:2/D 15:0 206 of Fig. 19), comprising: informing a start address (i.e., the step S211- A 1:0 & A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 20) required for data access (i.e., data reading) when said data access is executed from said primary board to said secondary boards (See Figs. 20 and 21); and generating an address (i.e., Start Address A 15:2 and Incremented Address A 1:0 in Figs. 20 and 22) used in said data access (i.e., Data 1-4 access in Fig. 20) in said primary board based on said start address (See page 5, lines 6-18).

AAPA does not teach said step of generating said address is performed in said secondary boards based on said start address, a predetermined trigger signal and a cycle signal indicating switching of data, said cycle signal is combined with said trigger signal.

Oshikawa discloses a method of performing data transfer at a high speed (See page 333, col. at right-lower, lines 9-19), wherein generating an address (i.e., memory address - address 65_U + address 65_L in Fig. 2) used in a data access in a secondary board (i.e., memory module 40 of Fig. 1; See page 334, col. at left-lower, lines 6-11) based on a start address (i.e., memory address 4A in Fig. 2; See page 335, col. at right-upper, lines 16-17), a predetermined trigger signal (i.e., counter signal 71 for a predetermined 1 byte transfer, counter signal 72 for a predetermined 2 bytes transfer or counter signal 73 for a predetermined 4 bytes transfer in Fig. 2; See page 335, col. at left-upper, line 6 through col. at left-lower, line 4) and a cycle signal (i.e., data enable signal 68 in Fig. 2) indicating switching of data (i.e., switching of D_{4A}, D_{4A+1}, D_{4A+2}, D_{4A+3}, etc. on Address/Data line 52 is indicated by a combined signal of said counter signal, low pulse, then said data enable signal, high pulse; See Fig. 2), said cycle signal is combined with said

trigger signal (i.e. data enable signal being combined with counter signal for accessing memory data in Fig. 2; See page 334, col. at left-lower, line 14 through page 335, col. at left-upper, line 5). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said step of generating said address used in said data access in said primary board, as disclosed by AAPA, by said step of generating an address used in a data access implemented in a secondary board (i.e., memory module), as disclosed by Oshikawa, for the advantage of providing a high speed data transfer (See Oshikawa, page 333, col. at right-lower, lines 18-19).

Referring to claim 3, Oshikawa teaches when said address (i.e., memory address - address 65_U+ address 65_L in Fig. 2) is generated based on said trigger signal (See timing diagram in Fig. 2; i.e., wherein in fact, memory address (i.e., address 65_U + address 65_L) is generated based on counter signal 71 for 1 byte transfer, counter signal 72 for 2 bytes transfer, or counter signal 73 for 4 bytes transfer in Fig. 2; See page 335, col. at left-upper, line 6 through col. at left-lower, line 4), said address is generated sequentially by incrementing said start address in response to a timing of said trigger signal (i.e., a timing of counter signal; See page 335, col. at left-upper, line 6 through col. at right-lower, line 2).

Referring to claim 5, AAPA discloses a data transmission system (Fig. 16) for carrying out data transmission/reception (See page 1, lines 16-20) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A 15:2/D 15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A 15:2/D 15:0 206 of Fig. 19), comprising: informing a memory start address (i.e., the step S211- A 1:0 & A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 20) of said secondary boards (i.e., Secondary board 200 including Memory 208 in Fig. 17) required for data access (i.e., data reading) when said data access is executed from said primary board to said secondary boards (See Figs. 20 and 21); judging in said secondary boards is

performing whether or not said memory start address is directed to own station (See page 2, line 25 through page 3, line 3; i.e., Separator 207 in Secondary Board 200 in Fig. 17 is performing the step S201 in Fig. 18), and then executing said data transmission via said data transmission path (i.e., data transmission bus) by accessing a memory (i.e., Memory 208 of Fig. 17) in own station (i.e., target Secondary Board 200 of Fig. 17) based on said memory start address when said memory start address is directed to own station (See page 3, lines 4-13 and Fig. 18); and generating an address (i.e., Start Address A 15:2 and Incremented Address A 1:0 in Figs. 20 and 22), to which said data transmission is subsequently executed (i.e., steps of S214-S220 in Fig. 20), in said primary board by incrementing said memory start address (i.e., incrementing A 1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 22) after said data transmission based on said memory start address is ended (i.e., steps of S211 and S212 in Fig. 20), and then executing said data transmission via said data transmission path by accessing said memory of own station (i.e., target Secondary Board) based on said generated address (See timing diagram in Fig. 22 and page 5, lines 6-18).

AAPA does not teach said step of generating said address is performed in said secondary boards, wherein a cycle signal indicating switching of data is used in combination with a trigger signal.

Oshikawa discloses a method of performing data transfer at a high speed (See page 333, col. at right-lower, lines 9-19), wherein generating an address (i.e., memory address - address 65_U + address 65_L in Fig. 2), to which a data transmission is subsequently executed (See page 334, col. at right-lower, line 7 through page 335, col. left-upper, line 5), in a secondary board (i.e., memory module 40 of Fig. 1; See page 334, col. at left-lower, lines 6-11) by incrementing a memory start address (i.e., memory address 4A in Fig. 2; See page 335, col. at right-upper, lines 16-17) after said data transmission based on said memory start address is ended (i.e., after the first data transmission D_{4A} based on the memory start address 4A in Fig. 2), and then executing said data transmission via a data transmission path by accessing a memory (i.e., memory 41 of Fig. 1) of own station (i.e., target memory module 40 in Fig. 1) based on

said generated address (See page 335, col. at left-upper, line 6 through col. at left-lower, line 4), wherein a cycle signal (i.e., data enable signal 68 in Fig. 2) indicating switching of data (i.e., enabling of data) is used in combination with a trigger signal (i.e. data enable signal being combined with counter signal for accessing memory data in Fig. 2; See page 334, col. at left-lower, line 14 through page 335, col. at left-upper, line 5; in fact, switching of D_{4A}, D_{4A+1}, D_{4A+2}, D_{4A+3}, etc. on Address/Data line 52 is indicated by a combined signal of said counter signal, low pulse, then said data enable signal, high pulse; See Fig. 2). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said step of generating said address used in said data transmission in said primary board, as disclosed by AAPA, by said step of generating an address used in a data transmission implemented in a secondary board (i.e., memory module), as disclosed by Oshikawa, for the advantage of providing a high speed data transfer (See Oshikawa, page 333, col. at right-lower, lines 18-19).

Referring to claim 6, AAPA discloses a data transmission system (Fig. 16) for carrying out data read (See page 1, lines 16-20 and page 3, lines 14+) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A 15:2/D 15:0 206 of Figs. 17 and 19) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A 15:2/D 15:0 206 of Fig. 19), comprising the steps of: informing a start address (i.e., the step S211- A 1:0 & A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 20) required for data read (i.e., data reading in Figs. 20 and 21) via said data transmission path (i.e., data transmission bus); switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 19); accessing a memory (i.e., Memory 208 of Fig. 17) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 19 and steps of S211-S214 in Fig. 20) and sending out a read result (i.e., Data 1 in step S214 in Fig. 20) onto said data transmission path (i.e., onto switched data

transmission bus at the step S213 in Fig. 20 as a Data Bus; See page 4, lines 8-12); and incrementing said start address (i.e., incrementing A 1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19), and then sending out a read result (i.e., Data 2-4 in steps S216, S218 and S220 in Fig. 20) onto said data transmission path (i.e., Data Bus) by accessing said memory based on said incremented address (See timing diagram in Fig. 19 and page 5, lines 6-18).

AAPA does not teach informing a trigger signal combined with a cycle signal indicating a timing of data access, and said step of incrementing said start address is executed at a timing of said trigger signal.

Oshikawa discloses a method of performing data transfer at a high speed (See page 333, col. at right-lower, lines 9-19), wherein informing a trigger signal (i.e., counter signal 71 for 1 byte transfer, counter signal 72 for 2 bytes transfer or counter signal 73 for 4 bytes transfer in Fig. 2; See page 335, col. at left-upper, line 6 through col. at left-lower, line 4) combined with a cycle signal (i.e., data enable signal 68 in Fig. 2) indicating a timing of data access (i.e., enabling signal for indicating data available; data enable signal being combined with counter signal for accessing memory data in Fig. 2; See page 334, col. at left-lower, line 14 through page 335, col. at left-upper, line 5), and incrementing said start address is executed at a timing of said trigger signal (i.e., a timing of counter signal; See page 335, col. at left-upper, line 6 through col. at right-lower, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said step of generating said address used in said data access in said primary board, as disclosed by AAPA, by said step of generating an address used in a data access implemented in a secondary board (i.e., memory module), as disclosed by Oshikawa, for the advantage of providing a high speed data transfer (See Oshikawa, page 333, col. at right-lower, lines 18-19).

Referring to claim 8, AAPA discloses a data transmission system (Fig. 16) for carrying out data write (See page 1, lines 16-20 and page 5, lines 21+) between a primary board (i.e., primary board 100 of Fig. 16 on the transmission transmitter side) and secondary boards (i.e., secondary boards A-C 200a-c in

Fig. 16 on the transmission receiver side) by using a data transmission path (i.e., data transmission bus 300 of Fig. 16), which employs a same signal line (A 15:2/D 15:0 (206) of Figs. 17 and 22) as an address bus (i.e., Address 15:2) and a data bus (i.e., Data 15:0) mutually (See timing diagram for A 15:2/D 15:0 (206) of Fig. 22), comprising the steps of: informing a start address (i.e., the step S241- A 1:0 & A15:2/D 15:0 START ADDRESS OUTPUT in Fig. 23) required for data write (i.e., data writing in Figs. 23 and 24) via said data transmission path (i.e., data transmission bus); switching said data transmission path to which said start address is informed as a data bus (See timing diagram A15:2/D15:0 (206) in Fig. 22), and then sending out a predetermined data (i.e., Data 1 in step S242 in Fig. 23) to be written to a memory (i.e., Memory 208 of Fig. 17); accessing said memory (i.e., Memory) based on said start address (i.e., ADDRESS of A15:2/D15:0 (206) and A1:0 (205) in Fig. 22 and steps of S241 and S242 in Fig. 23), and then writing said predetermined data to be written to a memory (See page 6, lines 6-16); and incrementing said start address (i.e., incrementing A 1:0 205 in sequence of 0h, 1h, 2h and 3h in Fig. 19), and then writing sequentially said predetermined data (i.e., Data 2-4 in steps S244, S246 and S248 in Fig. 23), that are sent out via said data transmission path (i.e., Data Bus), into said memory by accessing said memory based on said incremented address (See timing diagram in Fig. 22 and page 6, line 17 through page 7, line 6).

AAPA does not teach informing a trigger signal combined with a cycle signal indicating a timing of data access, and said step of incrementing said start address is executed at a timing of said trigger signal.

Oshikawa discloses a method of performing data transfer at a high speed (See page 333, col. at right-lower, lines 9-19), wherein informing a trigger signal (i.e., counter signal 71 for 1 byte transfer, counter signal 72 for 2 bytes transfer or counter signal 73 for 4 bytes transfer in Fig. 2; See page 335, col. at left-upper, line 6 through col. at left-lower, line 4) combined with a cycle signal (i.e., data enable signal 68 in Fig. 2) indicating a timing of data access (i.e., enabling signal for indicating data available; data enable signal being combined with counter signal for accessing memory data in Fig. 2; See page 334, col. at left-

lower, line 14 through page 335, col. at left-upper, line 5), and incrementing said start address is executed at a timing of said trigger signal (i.e., a timing of counter signal; See page 335, col. at left-upper, line 6 through col. at right-lower, line 2).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said step of generating said address used in said data access in said primary board, as disclosed by AAPA, by said step of generating an address used in a data access implemented in a secondary board (i.e., memory module), as disclosed by Oshikawa, for the advantage of providing a high speed data transfer (See Oshikawa, page 333, col. at right-lower, lines 18-19).

Response to Arguments

6. Applicant's arguments filed on 24th of September 2004 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "Oshikawa teaches incrementing the address using the count signal and the data enable. In Oshikawa, however, there is a possibility that the address is erroneously incremented due to the deformation of the wave of the count signal during data enabling, which is caused by external noise or signal reflection. In other words, Oshikawa fails to teach or suggest not incrementing or generating an address during the time in which the waveform is deformed by the count signal or noise. That is, Oshikawa fails to teach or suggest using a cycle signal indicating the switching of data in combination with the trigger signal. In Oshikawa, there is no cycle signal used in combination with the trigger signal that would indicate the switching to the previous data while alternating L/H for each switching of data. As a result, Oshikawa cannot prevent the occurrence of erroneous count up of the address when noise or reflection is overlapped on the count signal. In short, Oshikawa fails to teach or suggest generating an address based on the trigger signal combined with a cycle signal that indicates switching of data. Oshikawa does not cure the deficient teachings of the APA. ..." on the Response page 12, line 17 through page 14, line 5, the Examiner respectfully disagrees.

In fact, it is noted that the features upon which applicant relies (i.e., not incrementing or generating an address during the time in which the waveform is deformed by the count signal or noise, and using a cycle signal) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Furthermore, in contrary to the Applicant's statement, Oshikawa suggests a cycle signal (i.e., data enable signal 68 in Fig. 2) used in combination with the trigger signal (i.e., counter signal in Fig. 2) that would indicate the switching to the previous data while alternating L/H for each switching of data (i.e. data enable signal being combined with counter signal for accessing memory data in Fig. 2; See Oshikawa, page 334, col. at left-lower, line 14 through page 335, col. at left-upper, line 5; in fact, switching of D_{4A}, D_{4A+1}, D_{4A+2}, D_{4A+3}, etc. on Address/Data line 52 is indicated by a combined signal of said counter signal, low pulse, then said data enable signal, high pulse; See Fig. 2). See Paragraph 5 of the instant Office Action, Claims 1, 3, 5, 6 and 8 rejection under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Oshikawa.

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H. Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
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